EE 618: CMOS Analog VLSI Design
Project 2(Report)

Devesh Kumar, 16D070044
Electrical Engineering, IIT Bombay

1. PART-1- LAYOUT

1.1 DRC

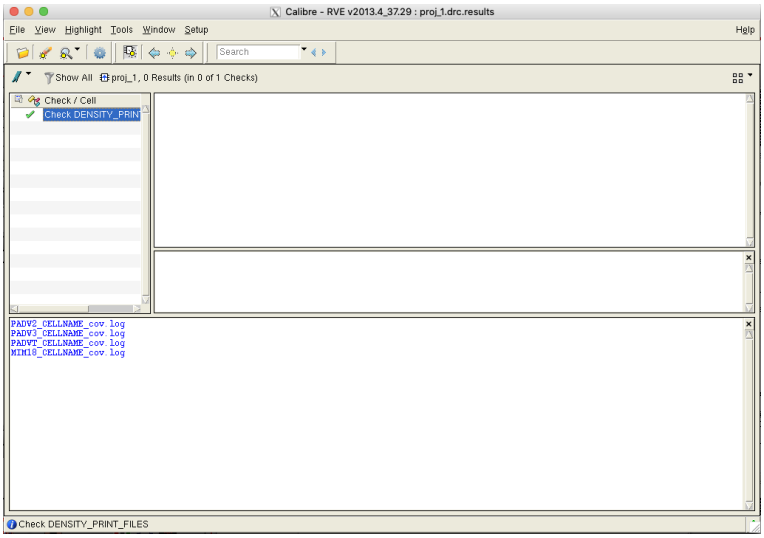

Figure 1. DRC

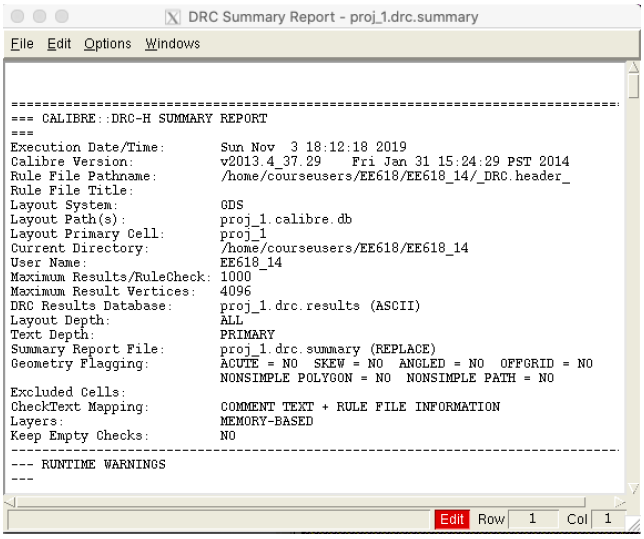

Figure 2. DRC

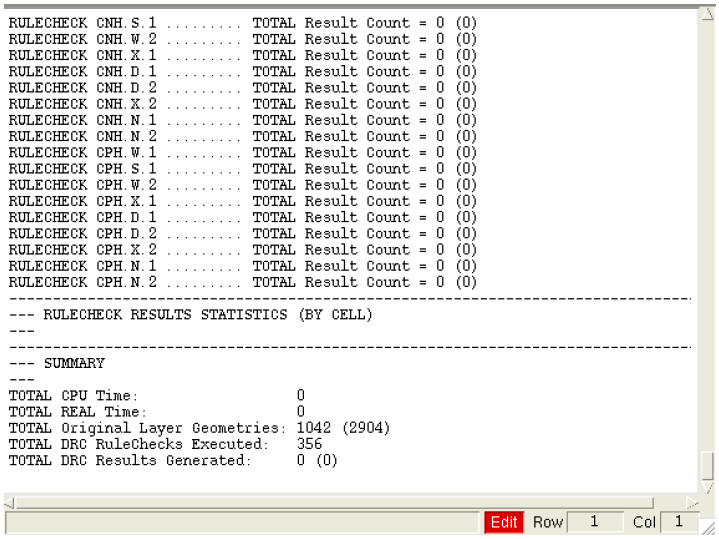

Figure 3. DRC

1.2 LVS

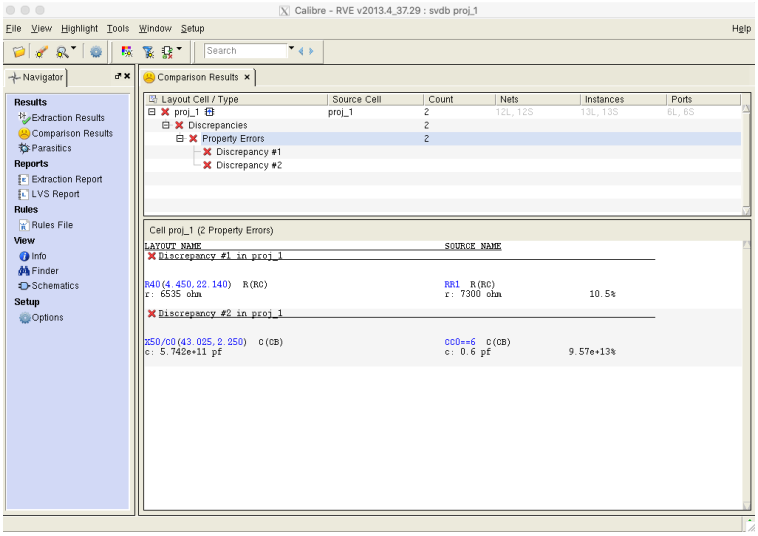

Figure 4. LVS

1.3 PEX

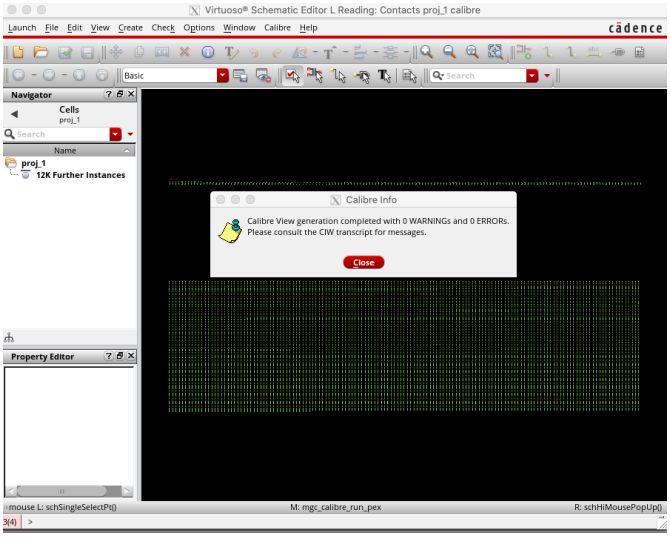

Figure 5. Pex

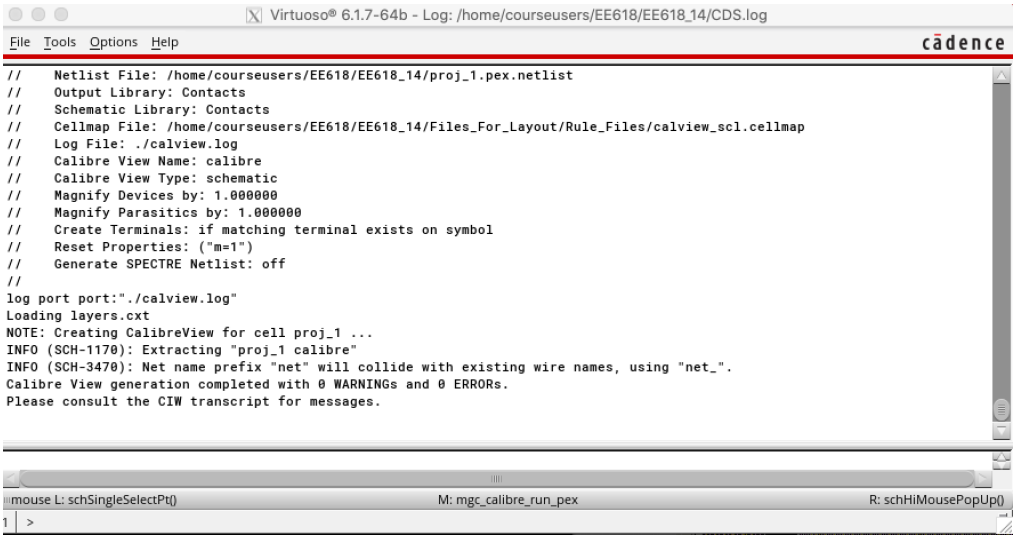

Figure 6. Pex

1.4 layout

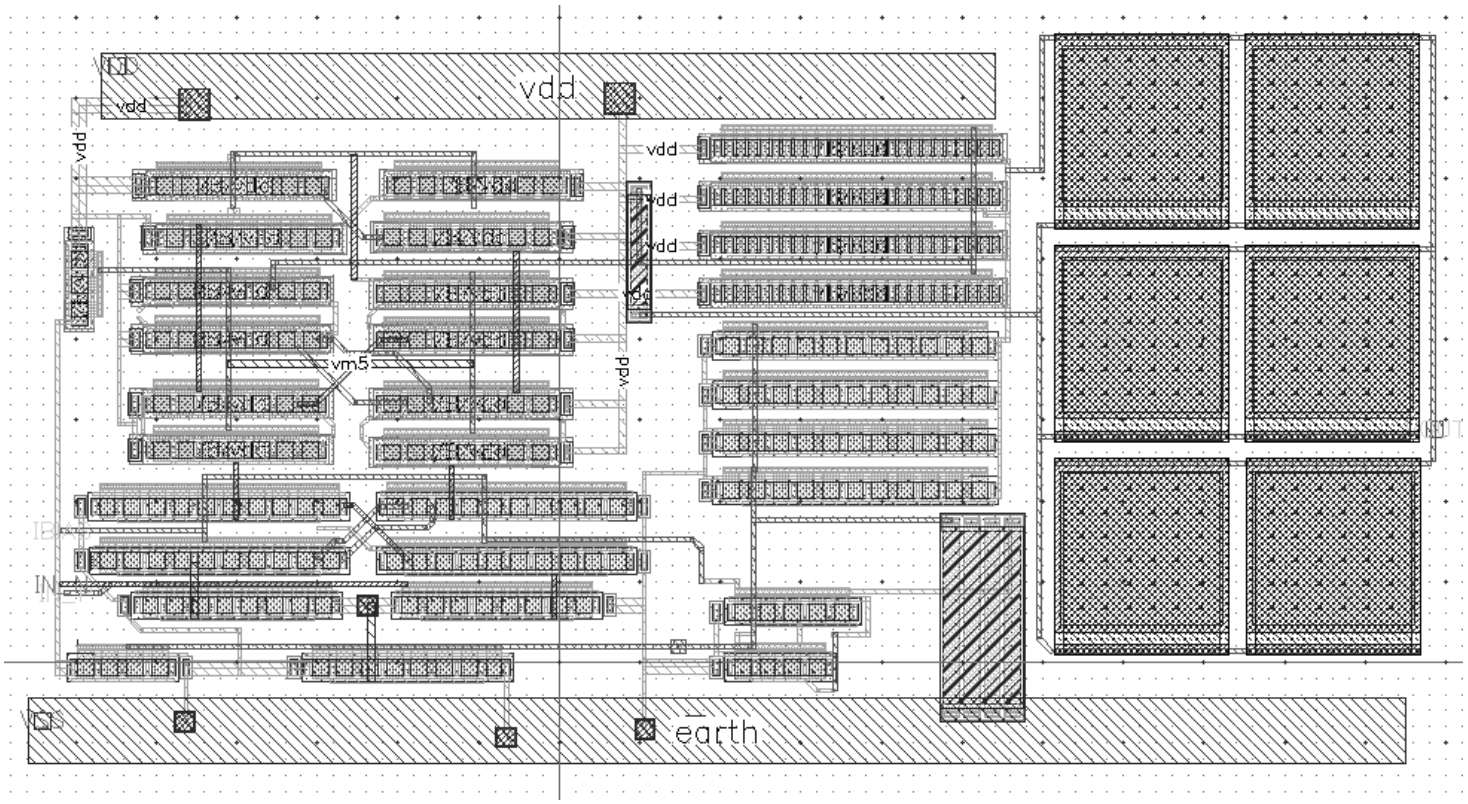

Figure 7. Layout

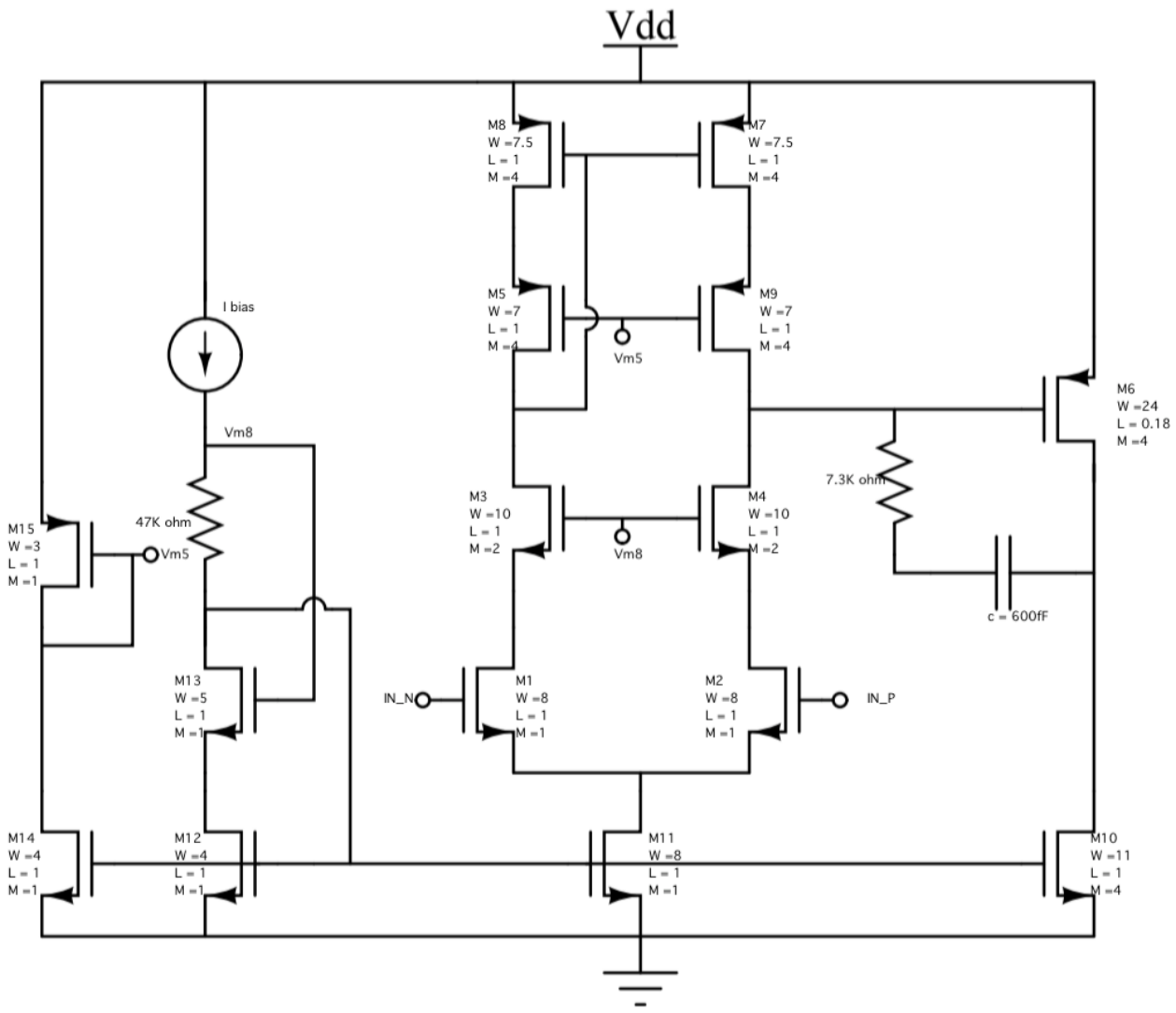

Figure 8. Schematic

2. PART-2-CHARACTERIZATION

2.1 STB Analysis

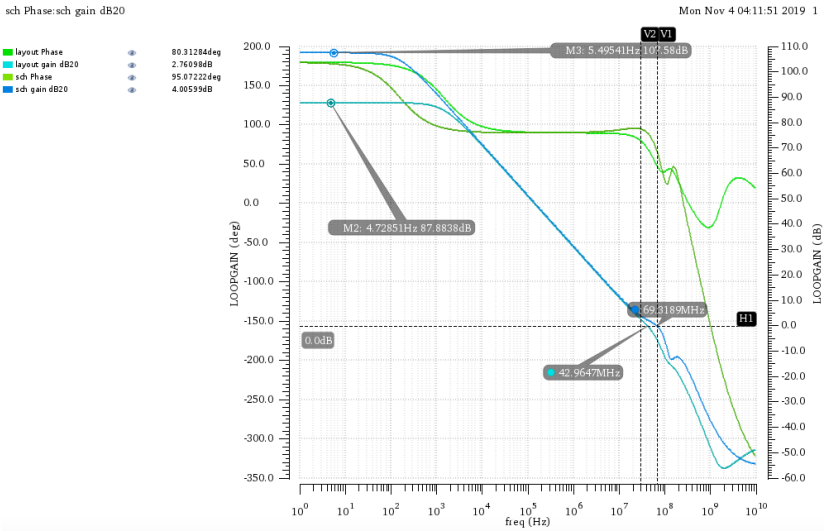

Figure 9. STB Analysis

Table 1. STB Specs Obtained

	Schematic	layout
DC gain	107db	87db
Unity gain Frequency	69.31Mhz	42.96Mhz
Phase Margin	66.75	70

For project 1 i had used the multipliers greater than 4. So i had to reduce so i introduced figure. So the results were little off tahn in the project 1.

2.2 Slew Rate

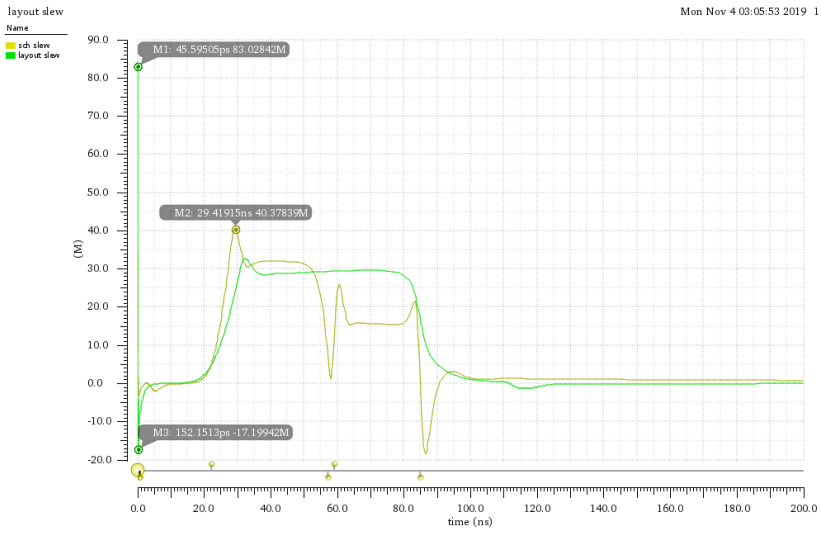

Figure 10. Slew rate

Table 2. Slew rate Specs Obtained

	Schematic	layout
Slew Rate	40.3V/μs	83.028V/μs

2.3 Settling time

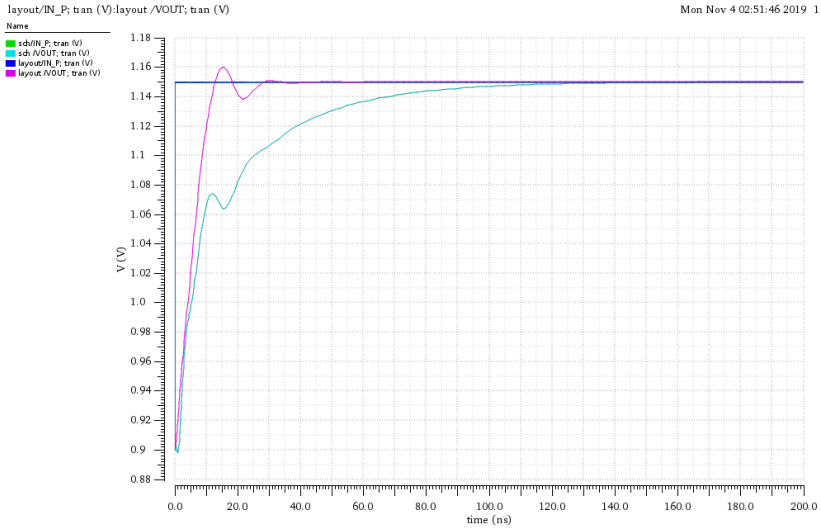

Figure 11. Settling Time

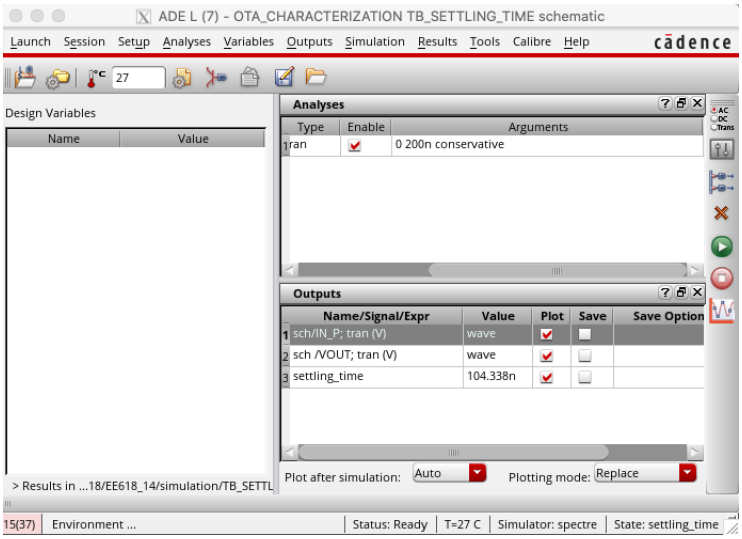

Figure 12. Settling time from From ADE (Schematic)

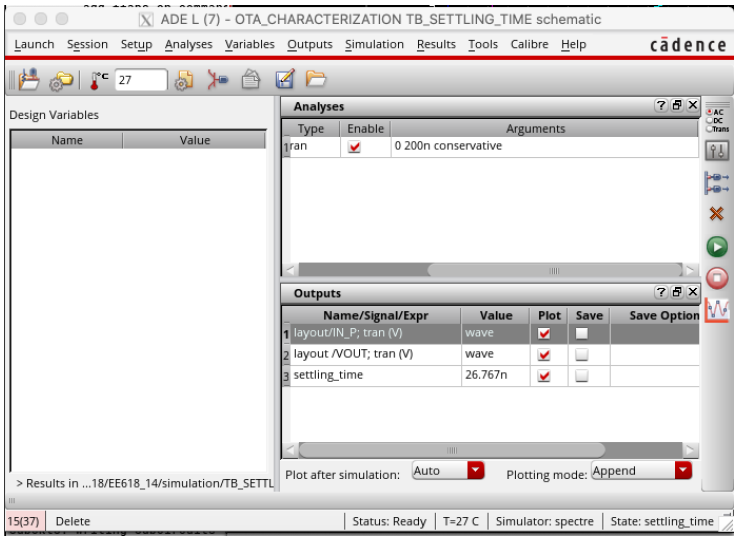

Figure 13. Settling time from From ADE (layout)

Table 3. Settling Time Specs Obtained

	Schematic	layout
Slew Rate	104ns	26.7ns

2.4 Systematic Offset

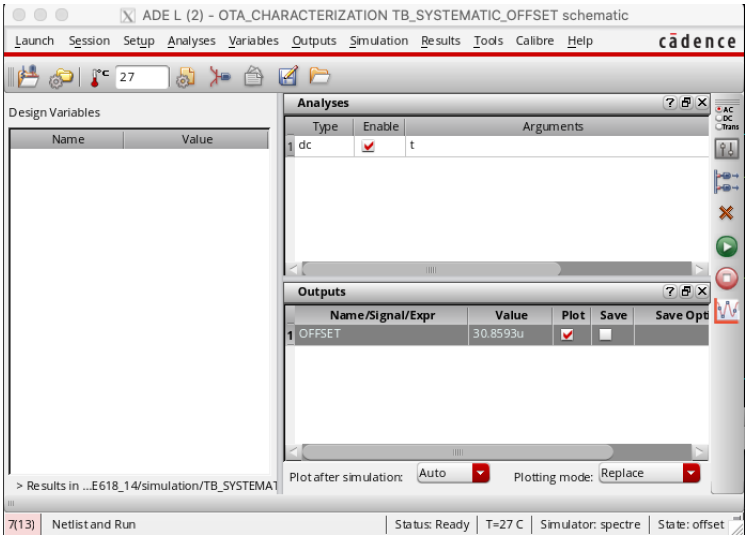

Figure 14. Offset from ADE

Table 4. Slew rate Specs Obtained

	Schematic	layout
Systematic offset	24.85 uV	30.85 uV

2.5 Noise

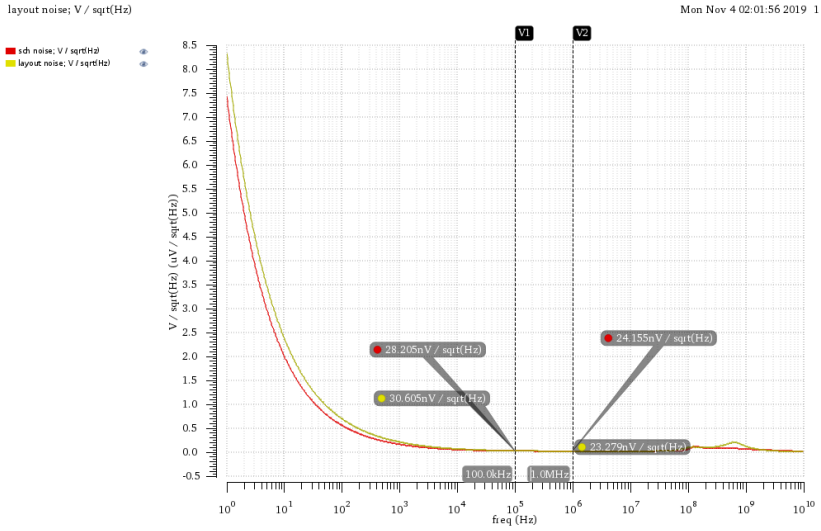

Figure 15. Input referred noise

Table 5. Noise Specs Obtained

	Schematic	layout
Input refered noise at 100Khz	$28.2V/hz^{0.5}$	$30.8V/hz^{0.5}$
Input refered noise at 1MHz	$24.1V/hz^{0.5}$	$23.2V/hz^{0.5}$

2.6 CMRR

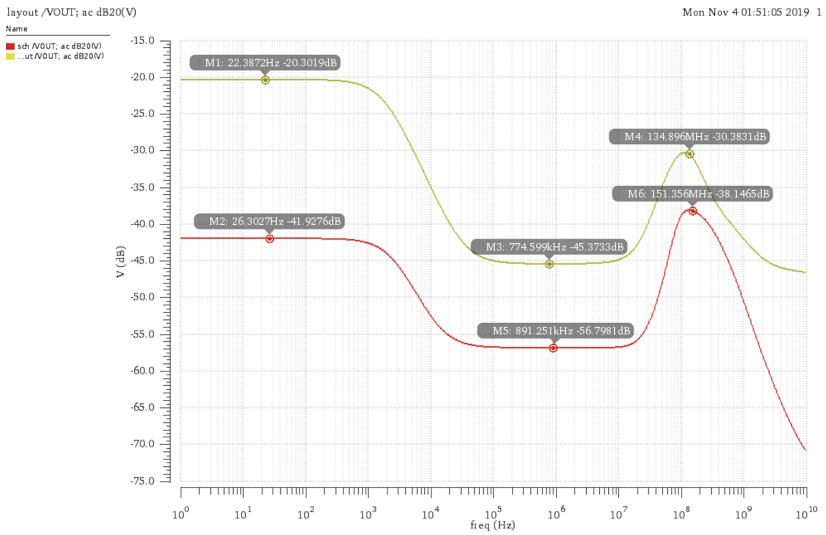

Figure 16. Common Mode Gain

Table 6. CMRR

	Schematic	layout
CMRR	107 - (-40) = 147db	88.8 - (-20.3) = 109.1db

2.7 PSRR

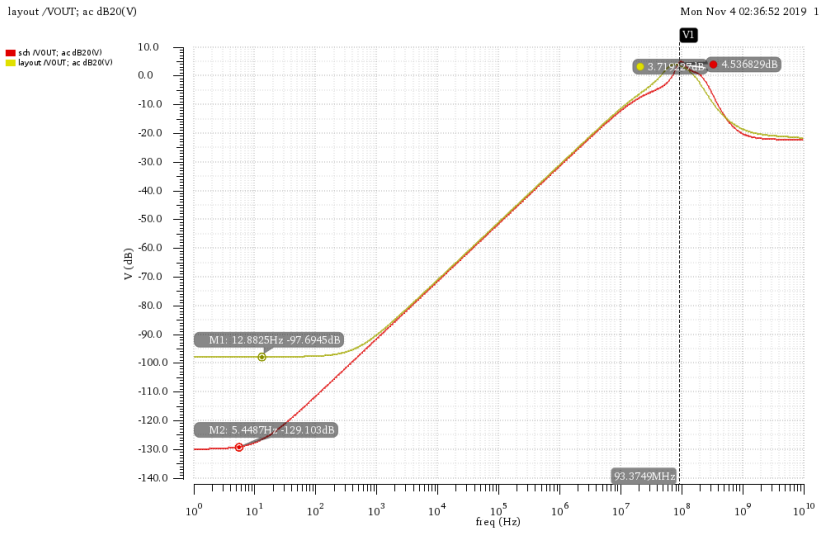

Figure 17. PSRR plus

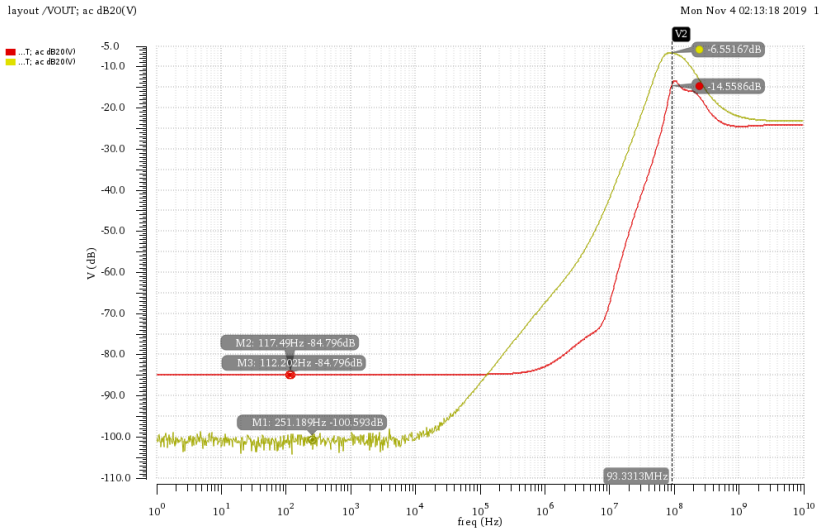

Figure 18. PSRR minus

Table 7. PSRR specs obtained

	Schematic	layout
PSRR plus	-129db	-97.69db
PSRR minus	-84.79db	100.593db

2.8 Input Common Mode Range

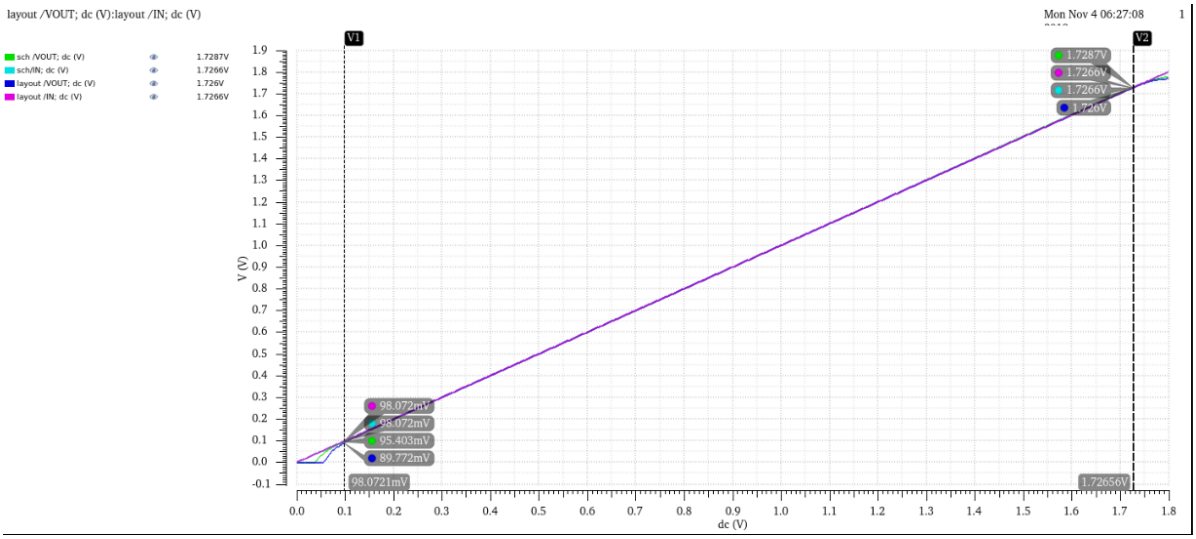

Figure 19. ICMR

2.9 Closed Loop gain

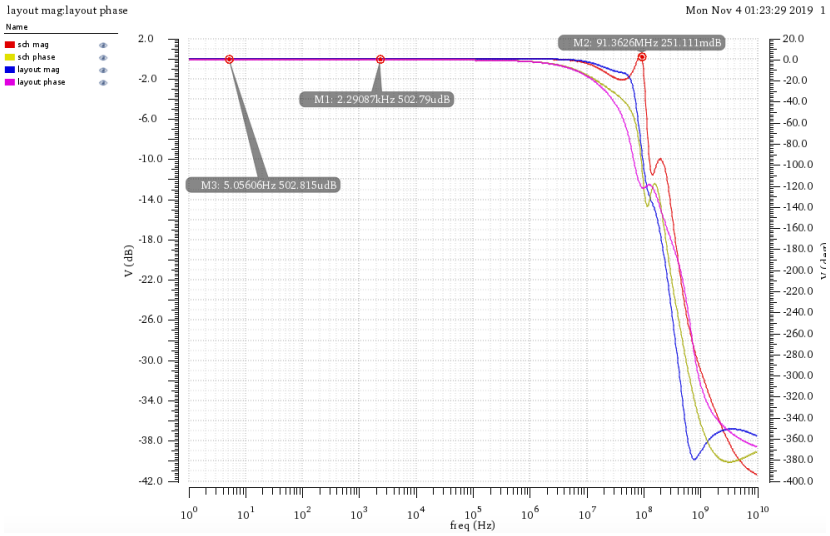

Figure 20. Closed loop gain

2.10 Closed Loop Transient Analysis

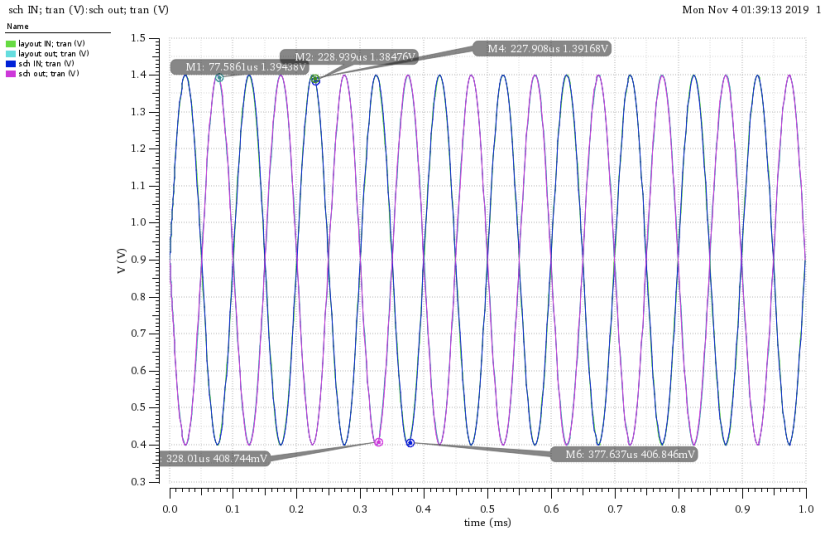

Figure 21. Closed loop Transient Analysis

2.11 SS

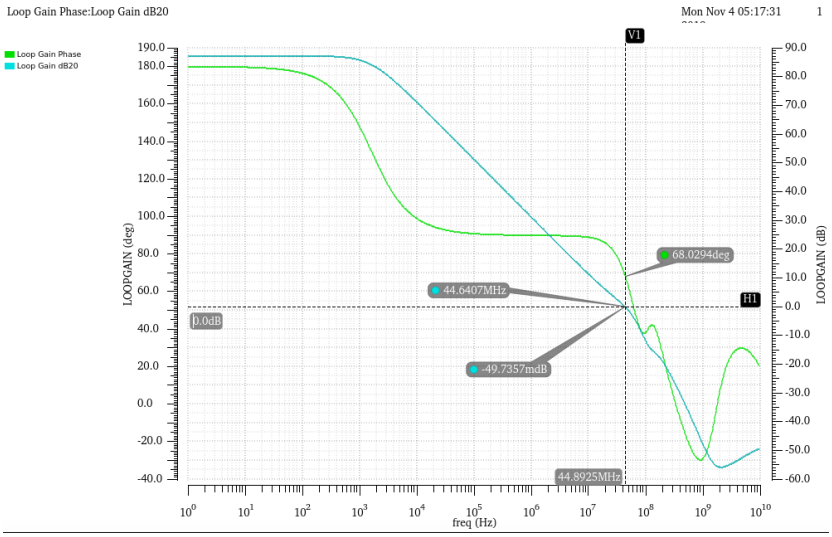

Figure 22. SS at 0C

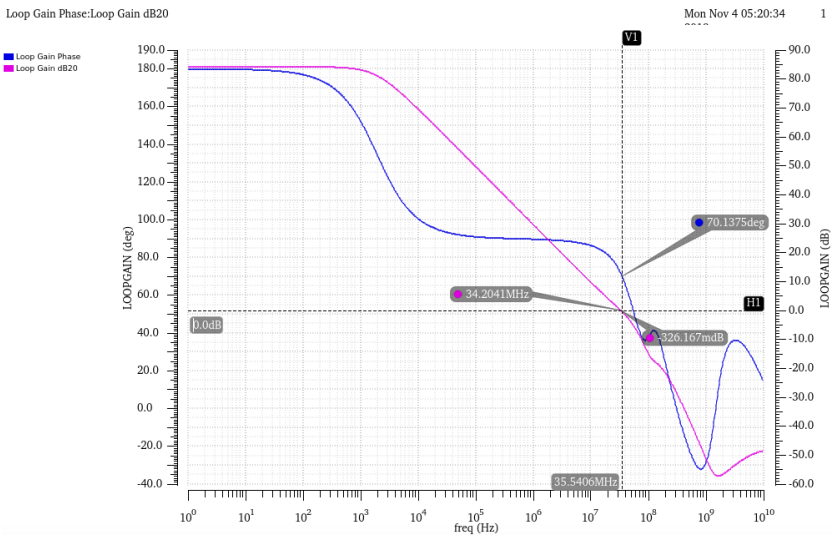

Figure 23. SS at 100C

2.12 FF

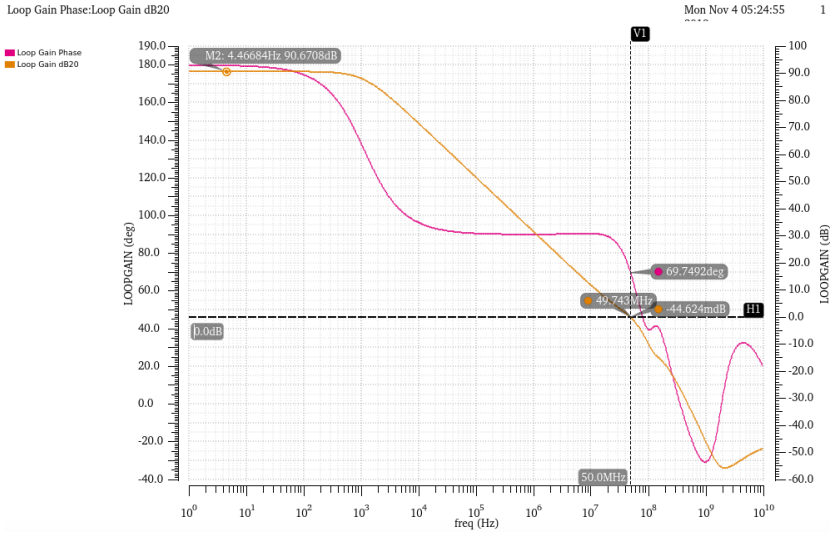

Figure 24. FF at 0C

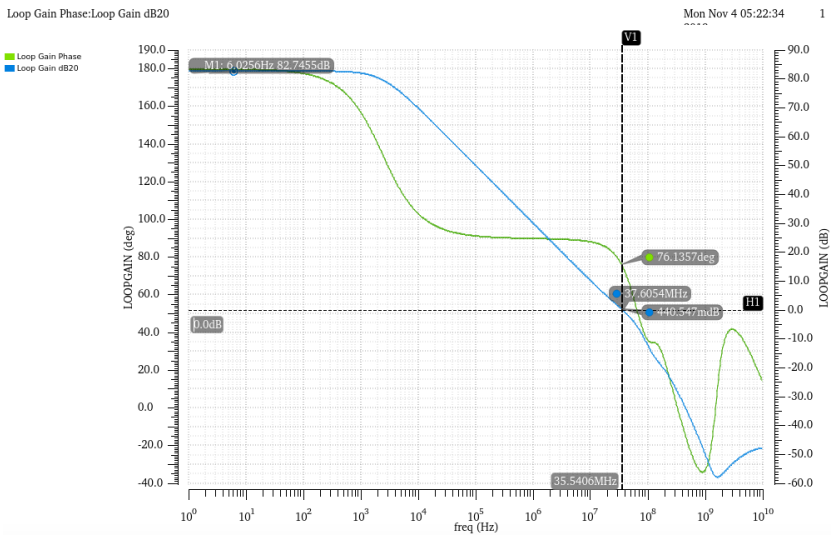

Figure 25. FF at 100C

3. COMPARISION

Table 8. Power consumption Specs Obtained

	Schematic	layout
DC gain	107dB	87db
Unity Gain frequency	69.31Mhz	42.96Mhz
Phase Margin	66.75	70
Slew rate	40.3V/us	83.028V/us
Output Swing (Vpp)	1V	1V
Settling Time (1 accuracy)	104ns	26.7 ns
Input referred spot noise (at 1 MHz)	$24.1V/hz^{0.5}$	23.2 $V/hz^{0.5}$
Input referred spot noise (at 100 KHz)	$28.2V/hz^{0.5}$	30.8 $V/hz^{0.5}$
CMRR	147db	109.1db
PSRR Pluse	-129db	-97.69 db
PSRR Minus	-84.79db	-100.593db
Power	275uW	275uW
Area	45.29um * 87.335um = 3,955.4 um*um	